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10/599,494	05/29/2007	Kozo Kimura	P30890	9808

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EXAMINER	
TORRENTE, RICHARD T	
ART UNIT	PAPER NUMBER
2485	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/599,494	KIMURA ET AL.	
	Examiner	Art Unit	
	RICHARD TORRENTE	2485	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2011*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 15 is objected to because of the following informalities: “processor includes has an instruction” is grammatically incorrect in line 3. Appropriate correction is required.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim(s) 1 and 3-25 is/are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 1 recites the limitation "said stream input/output block" in line 2, page 3. There is insufficient antecedent basis for this limitation in the claim.

4. Claim 17 recites the limitation "said stream input/output block" in line 5. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3-5, 9, 11-21, 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Owen et al. (US 7,321,368 B2) in view of Yamada et al. (US 2002/0023237 A1).

Regarding claim 1, Owen discloses an integrated circuit for video/audio processing that processes video and audio signals (see abstract), comprising: a microcomputer including a CPU (central processing unit) (see 152 in fig. 3); a stream input/output (see 186 in fig. 3) operable to receive/output a video and audio stream (e.g. see output of 166 in fig. 3) to and from an external device (e.g. see 166 in fig. 3), under a control of said microcomputer; a media processor (see 80 in fig. 3) operable to execute media processing including at least one of compression and decompression (see 44 and 46 in fig. 2 and fig. 3) of the video and audio stream inputted to said stream input/output or outputted from said stream input/output under the control of said microcomputer; an AV input/output (see 200 and 180 in fig. 3) operable to convert the video and audio stream subjected to the media processing in said media processor and output the video and audio stream to a first external apparatus (e.g. see 182 and 176 in

fig. 3), or acquire the video and audio signal from a second external apparatus (e.g. see 164 in fig. 3) and convert the video and audio signal into a video and audio stream subjected to the media processing in said media processor, under the control of said microcomputer (see 152, 200, 180, 190 and 80 in fig. 3); and a memory interface (see 72 and 76 in fig. 3) operable to control a data transfer between a memory (e.g. see 168 in fig. 3) and said microcomputer, said stream input/output block, said media processor and said AV input/output, under the control of said microcomputer (see interconnections in fig. 3).

Although Owen discloses each of said microcomputer, said stream input/output, said media processor and said AV input/output is connected to said memory interface by each of respective plural data buses (see interconnections in fig. 3), each of the respective plural data buses is associated to one of said microcomputer, said stream input/output, said media processor and said AV input/output (see interconnections in fig. 3), and the video and audio stream is exchanged through said memory among said microcomputer, said stream input/output, said media processor and said AV input/output (see interconnections in fig. 3), it is noted that Owen does not disclose wherein the each of respective plural data buses are dedicated data buses

However, Yamada, in the same field of endeavor, discloses an integrated circuit setup wherein each processing block (e.g. see 401 in fig. 9) is connected to a memory interface (see 402 in fig. 9) by each of respective plural dedicated data buses (see fig. 9).

Given the teachings as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Yamada teachings of dedicated buses into Owen buses for the benefit of saving power consumption by providing an exclusive operational mode apart from normal operational mode, wherein the operational mode is for short-term direct access of one device without powering up other devices.

Regarding claim 3, Owen further discloses wherein said memory interface is operable to relay the data transfer so that the data transfer between said memory and said microcomputer, said stream input/output, said media processor and said AV input/output is made in parallel (e.g. see 72 and 76 in fig. 3).

Regarding claim 4, Owen further discloses wherein said microcomputer, said stream input/output, said media processor and said AV input/output have no buffer memory for buffering the video and audio stream (see fig. 3).

Regarding claim 5, Owen further discloses wherein said microcomputer, said stream input/output, said media processor and said AV input/output store the video and audio stream in said memory and notifies remaining ones of said stream input/output, said media processor and said AV input/output of the storage (see 152, 72, 76 and 168 in fig. 3).

Regarding claim 9, Owen further discloses comprising: a signal line (see line between 72 and 82) which connects said stream input/output and said media processor, wherein said media processor is operable to execute media processing of the video and audio stream inputted from said stream input/output block through said signal line or the video and audio stream to be outputted to said stream input/output through said signal line (see 72 and 80 in fig. 3).

Regarding claims 11 and 18, Owen further discloses wherein a structure of said integrated circuit is included in each of plural different system LSI (large-scale integration) corresponding to each of (see 190 in fig. 3) plural different devices; and the plural different devices include at least two among a digital television (see 182 in fig. 3), a digital video recorder, a video camera and a portable telephone (se column 9, line 32).

Regarding claims 12 and 19, Owen further discloses wherein assuming that one of said plural different devices is designated as a first device (see 166 in fig. 3) and another as a second device (see 164 in fig. 3) and a process is shared by said integrated circuit for video/audio processing for the first device and said integrated circuit for video/audio processing for the second device (see 190 with 164 and 166 in fig. 3); in the case where the process is executed by said microcomputer of said integrated circuit for video/audio processing for the first device, the process is executed by said microcomputer of said integrated circuit for video/audio processing for the second device (see 152 in fig. 3); in the case where the process is executed by said

stream input/output of said integrated circuit for video/audio processing for the first device, the process is executed by said stream input/output of said integrated circuit for video/audio processing for the second device (see 186 in fig. 3); in the case where the process is executed by said media processor of said integrated circuit for video/audio processing for the first device, the process is executed by said media processor of said integrated circuit for video/audio processing for the second device (see 80 in fig. 3); and in the case where the process is executed by said AV input/output of said integrated circuit for video/audio processing for the first device, the process is executed by said AV input/output of said integrated circuit for video/audio processing for the second device (see 200 in fig. 3).

Regarding claim 13, Owen discloses wherein in the case where one of the plural different devices is designated as a first device and another as a second device (see column 9, lines 32-65, wherein it is implied that two user of fig. 3 will have separate device), wherein the CPU of said integrated circuit for video/audio processing for the first device and the CPU of said integrated circuit for video/audio processing for the second device have instruction sets partially compatible (e.g. H.261 in column 9, lines 32-34) with each other (see 80 in fig. 3).

Regarding claim 14, Owen further discloses wherein said media processing includes an instruction parallel processor which executes plural signal processing instructions in parallel (see 52 to 44 and 46 in fig. 3); and in the case where one of the

plural different devices is designated as a first device and another as a second device (see column 9, lines 32-65, wherein it is implied that two user of fig. 3 will have separate device), the instruction parallel processor of said integrated circuit for video/audio processing for the first device and the instruction parallel processor of said integrated circuit for video/audio processing for the second device have instruction sets partially compatible with each other (see compatible mpeg coding/decoding in column 9, lines 32-34).

Regarding claim 15, Owen further discloses wherein said media processor includes has an instruction parallel processor which executes plural signal processing instructions in parallel (see 52 to 44 and 46 in fig. 3); and in the case where one of the plural different devices is designated as a first device and another as a second device (see column 9, lines 32-65, wherein it is implied that two user of fig. 3 will have separate CPU), a core of the CPU of said integrated circuit for video/audio processing for the first device and the core of a CPU of said integrated circuit for video/audio processing for the second device have a same logic connection (see fig. 3), and a core of the instruction parallel processor of said integrated circuit for video/audio processing for the first device and a core of the instruction parallel processor of said integrated circuit for video/audio processing for the second device have a same logic connection (see fig. 3).

Regarding claim 16, Owen further discloses wherein said media processor includes an instruction parallel processor which executes plural signal processing

instructions in parallel (see 52 to 44 and 46 in fig. 3); and in the case where one of the plural different devices is designated as a first device and another as a second device (see column 9, lines 32-65, wherein it is implied that two user of fig. 3 will have separate CPU), a core of the CPU of said integrated circuit for video/audio processing for the first device and a core of the CPU of said integrated circuit for video/audio processing for the second device have a same mask layout (see fig. 3), and a core of the instruction parallel processor of said integrated circuit for video/audio processing for the first device and a core of the instruction parallel processor of said integrated circuit for video/audio processing for the second device have a same mask layout (see fig. 3).

Regarding claim 17, Owen further discloses wherein in the case where one of the plural different devices is designated as a first device and another one is designated as a second device (see column 9, lines 32-65, wherein it is implied that two user of fig. 3 will have separate CPU), an address of a control register for said stream input/output block, said media processor, said AV input/output and said memory interface on a memory map of the CPU in said integrated circuit for video/audio processing for the first device is identical to an address of a control register for said stream input/output, said media processor, said AV input/output and said memory interface on a memory map of the CPU in said integrated circuit for video/audio processing for the second device (column 11, lines 28-44).

Regarding claim 20, Owen further discloses wherein said AV input/output is further operable to generate a recording video signal by converting a resolution (see 200 in fig. 3) of a video signal converted from the video stream subjected to media processing by said media processor or acquired from said second external apparatus, as well as generating field feature information (see column 11, lines 47-51) indicating at least one of in-field total (see column 3, lines 14-19) and inter-field difference of video fields indicated by the recording video signal (see column 9, lines 7-10); and said media processor is further operable to access the field feature information and convert the recording video signal into a recording video stream (see 166 in fig. 3).

Regarding claim 21, Owen further discloses comprising a signal line (see interconnection between 200 and 80 in fig. 3) which connects said media processor and said AV input/output, wherein the field feature information is exchanged between said media processor and said AV input/output through said signal line (see column 11, lines 47-51 and 80 in fig. 3).

Regarding claim 24, the claim(s) recite analogous limitations to claim 1, and is/are therefore rejected on the same premise.

Regarding claim 25, the claim(s) recite analogous limitations to claim 1, and is/are therefore rejected on the same premise.

3. Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Owen et al. (US 7,321,368) in view of Yamada et al. (US 2002/0023237 A1), and further in view of O'Sullivan (US 2005/0235134).

Regarding claims 6 and 7, Owen further discloses wherein said stream input/output includes an interface (see 186 in fig. 3) operable to transmit and receive the video and audio stream to and from said external device, an encryption processor (see 80 and 180 in fig. 3) operable to encrypt or decrypt the transmitted and received video and audio stream, and a first direct memory access controller (see 52 and 60 in fig. 2) operable to transfer data between said external device and said memory, said media processor including an instruction parallel processor (see 52 to 44 and 46 in fig. 3) which executes plural signal processing instructions in parallel, and a second direct memory access controller (see 52 in fig. 3) operable to control the data transfer with said memory, said AV input/output includes a graphics engine (see 200 in fig. 3) which executes graphics processing of image data, and a format converter (see 200 in fig. 3) operable to convert the format of the video signal, and said memory interface includes plural ports (see 72 and 76 in fig. 3) connected to said microcomputer, said stream input/output, said media processor and said AV input/output, and has a memory scheduler (see 156, 154 and 82 in fig. 3) which adjusts timing of data transfer at each of said plural ports.

Although Owen discloses decoding and encoding (see 80 in fig. 3) and control (see 156, 154 and 82 in fig. 3), it is noted that Owen and Yamada do not disclose an accelerator which executes an arithmetic operation; wherein said microcomputer further includes at least one of a clock controller operable to turn on/off a supply of a clock to said CPU and a power supply controller operable to turn on/off the power supply.

However, O'Sullivan, in the same field of endeavor, discloses an optimizing processor wherein an accelerator (see ¶ [0083]) which executes an arithmetic operation; wherein said microcomputer further includes at least one of a clock controller operable to turn on/off a supply of a clock to said CPU and a power supply controller operable to turn on/off the power supply (see ¶ [0097]).

Given the teachings as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate O'Sullivan teachings of processor optimization into Owen and Yamada parallel processor for the benefit of increasing processing efficiency and reducing power consumption.

Regarding claim 8, Owen and Yamada, now incorporating the teaching of O'Sullivan, further discloses wherein said media processing block further has a data parallel processor which executes an arithmetic operation on plural pieces of data in parallel (see Owen 80 in fig. 3 and O'Sullivan ¶ [0083]).

4. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Owen et al. (US 7,321,368) in view of Yamada et al. (US 2002/0023237 A1), and further in view of Yamazaki (US 2004/0079952).

Regarding claim 10, although Owen discloses the blocks, it is noted that Owen and Yamada do not disclose wherein circuit elements and wiring between said microcomputer, said stream input/output, said media processor, said AV input/output and said memory interface are formed on a circuit layer and a first wiring layer, respectively, on a semiconductor substrate; and each of said plural dedicated data buses is formed on a second wiring layer located above said first wiring layer.

However, Yamazaki, in the same field of endeavor, discloses a semiconductor fabrication wherein circuit elements and wiring between the circuit elements in said microcomputer block, said stream input/output block, said media processing block, said AV input/output block and said memory interface block are formed on a circuit layer and a first wiring layer, respectively, on a semiconductor substrate; and said data bus is formed on a second wiring layer located above said first wiring layer (see 717, 719 and 720 in fig. 9D).

Given the teachings as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Yamazaki teachings of block layers into Owen and Yamada blocks for the benefit of decreasing the bulk defect density and interface defect density formed in a crystalline semiconductor layer.

5. Claims 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Owen et al. (US 7,321,368) in view of Yamada et al. (US 2002/0023237 A1), and further in view of Smith (US 2005/0053028).

Regarding claim 22, Owen further discloses wherein said media processor executes, a video data compressing or decompressing process (see 80 in fig. 3), and an audio data compressing or decompressing process for one video/audio multiplex stream (see 80 and 180 in fig. 3).

Although Owen discloses multiplexing or demultiplexing process (e.g. see 166 separated to 12 and 14 in fig. 2) for the video and audio stream, it is noted that Owen and Yamada do not disclose a time division, a multiplexing or demultiplexing process for the stream, as well as prohibiting the multiplexing or demultiplexing process for the video and audio stream from being executed plural times within a predetermined time.

However, Smith, in the same field of endeavor, discloses a data protocol wherein a time division, a multiplexing or demultiplexing process for the video and audio stream (see ¶ [0004]), as well as prohibiting the multiplexing or demultiplexing process for the video and audio stream from being executed plural times within a predetermined time (see ¶ [0023]).

Given the teachings as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Smith teachings of time division into Owen and Yamada division for the benefit of a gateway and protocol which

is capable of efficiently switching data between and among the circuit domain and the packet domain.

Regarding claim 23, Owen further discloses wherein said media processor includes a virtual multiprocessor functioning as plural logical processors (see 80, 158, 180, 200 in fig. 3) the compressing or decompressing process for said video data (see 80 in fig. 3), and the compressing or decompressing process for said audio data are executed by different logical processors (see 200 and 180 in fig. 3), respectively, which are a function of said virtual multiprocessor;

Although Owen discloses multiplexing or demultiplexing process (e.g. see 166 separated to 12 and 14 in fig. 2) for the video and audio stream, it is noted that Owen and Yamada do not disclose a time division, a multiplexing or demultiplexing process for the stream, and the logical processor for executing the multiplexing or demultiplexing process for said video and audio stream sleeps until an expiration of a time on a predetermined timer after completion of the processing of a predetermined unit of said video and audio stream.

However, Smith, in the same field of endeavor, discloses a data protocol wherein a time division, a multiplexing or demultiplexing process for the video and audio stream (see ¶ [0004]), and the logical processor for executing the multiplexing or demultiplexing process for said video and audio stream sleeps until an expiration of the time on a predetermined timer after completion of the processing of a predetermined unit of said video and audio stream (see ¶ [0023]).

Given the teachings as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Smith teachings of time division into Owen and Yamada division for the benefit of a gateway and protocol which is capable of efficiently switching data between and among the circuit domain and the packet domain.

Response to Arguments

1. Applicant's arguments with respect to claims 1 and 3-25 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

1. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RICHARD TORRENTE whose telephone number is (571) 270-3702. The examiner can normally be reached on M-Th: 7:30 - 6:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Richard Torrente/
Examiner, Art Unit 2485

/Jayanti K. Patel/
Supervisory Patent Examiner, Art Unit 2485

April 14, 2011